Remarks

Claims 1-5 and 7-18 are currently pending in the patent application. For the reasons and arguments set forth below, Applicant respectfully submits that the claimed invention is allowable over the cited references.

The instant Office Action dated July 31, 2007, requests that Figures 1A, 1B, and 3B be designated as Prior Art, and lists the following objection and rejections: claims 7 and 8 are objected to due to grammatical errors; claims 1-18 stand rejected under 35 U.S.C. 112(2); claims 1-3 and 5-18 stand rejected under 35 U.S.C. 102(b) over Matsushita *et al.* (U.S. Patent No. 5,323,041); and claim 4 stands rejected under 35 U.S.C. 103(a) over Matsushita *et al.*

Regarding the Office's Action's request that Figures 1A, 1B, and 3B be designated as Prior Art, Applicant has label these Figures as Prior Art as indicated on page 2 of this paper.

Regarding the objection to claims 7 and 8, Applicant has amended these claims to correct typographical errors. Thus, Applicant requests that the objection to claims 7 and 8 be removed.

Applicant respectfully traverses the Section 112(2) rejection of claims 1-18 because the claims do particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Applicant submits that the term "region" is commonly used in claiming semiconductor devices as is evidenced by the usage of the term in numerous issued patents including the Matsushita reference upon which the Office Action relies. It appears that the Office Action is attempting to limit the breadth of the claims by improperly asserting indefiniteness because the claims are not worded as the Office Action would prefer. Such an assertion is contrary to M.P.E.P. § 2173.04 because the "(b)readth of a claim is not to be equated with indefiniteness." See In re Miller, 441 F.2d 689 (CCPA 1971). Thus, the usage of the term "region" does not render the claims indefinite because one of skill in the art would be reasonably apprised as to the scope of the invention. See, e.g., M.P.E.P. § 2171. Regarding claim 9, Applicant submits that antecedent basis for the p and n semiconductor regions can be found in claim 1 at line 2. Therefore, the Section 112(2) rejection of claims 1-18 is improper and Applicant requests that it be withdrawn.

Applicant respectfully submits that the Section 102(b) rejection of claims 1-3 and 5-18 cannot stand because the cited portions of the Matsushita reference do not correspond to the claimed invention which includes, for example, aspects directed to the field shaping region being located adjacent only one of the p and n semiconductor regions that form the pn junction. The Office Action cites to the junction between p layer 2 and n layer 1, to insulation films 8 and 13, and to electrodes 4 and 5 as corresponding to Applicant's pn junction, field shaping region and capacitive voltage coupling regions respectively. *See, e.g.*, Matsushita's Figure 6. However, the Matsushita reference teaches that insulating films 8 and 13 are located adjacent both p layer 2 and n layer 1. *See, e.g.*, Figures 5 and 6. Matsushita further teaches, in certain embodiments, that the insulating film 13 includes films 13₁, 13₂ and 13₃, but the insulation films 13₁, 13₂ and 13₃ do not extend from one of the electrodes 4 and 5 to the other. *See, e.g.*, Figures 4 and 7. Thus, the cited portions of Matsushita do not correspond to Applicant's field shaping region. Accordingly, the Section 102(b) rejection of claims 1-3 and 5-18 is improper and Applicant requests that it be withdrawn.

Applicant further traverses the Section 102(b) rejection of claims 14-18 because these claims do not recite the intended use of the device as asserted by the Office Action. These claims recite structural features that have been improperly ignored by the Office Action. For example, claim 14 recites that the device is a diode and the pn junction is the rectifying junction of the diode. In another example, claim 16 recites that the device is a field effect transistor. These claims state what the device is (*i.e.*, structure), not how the device is used (*i.e.*, function). For instance, one of skill in the art would recognize the structure of a diode and a FET without using the diode or the FET. Accordingly, these limitations cannot be properly construed as having only functional characteristics as the use of the corresponding structure is not necessary to identify the structure. Therefore, the Section 102(b) rejection of claims 14-18 is improper and Applicant requests that it be withdrawn.

Applicant respectfully traverses the Section 103(a) rejection of claim 4 based upon the Matsushita reference because the cited portions of Matsushita do not correspond to the claimed invention as discussed above in relation to the Section 102(b) rejection of claim 1. In at least this regard, the Section 103(a) rejection of claim 4 is improper

because this claim depends from claim 1. Therefore, Applicant requests that the Section 103(a) rejection of claim 4 be withdrawn.

Regarding the Office Action's comments on page 2 concerning the inventorship of the instant application, Applicant believes that the Declaration properly listed the three inventors as did the initial Transmittal Letter filed on 11/14/05. Applicant further believes that the USPTO incorrectly listed only one inventor on the Filing Receipt mailed on 1/19/07 and on U.S. Patent Application Publication No. 2007/0090470 published on 4/26/07. Applicant requests that any future correspondence correctly list all three inventors. In the event that the Office Action is asserting that there is some problem concerning the inventorship of the instant application, clarification is respectfully requested.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063 (or the undersigned).

Please direct all correspondence to:

Corporate Patent Counsel NXP Intellectual Property & Standards 1109 McKay Drive; Mail Stop SJ41 San Jose, CA 95131

CUSTOMER NO. 65913

Name: Robert J. Crawford

Reg. No.: 32,122 651-686-6633 (NXPS.320PA)

Attachments: Two Replacement Drawing Sheets